

Course Handout

Course Number : **EEE ZG512**
Course Title : **EMBEDDED SYSTEM DESIGN**
Instructor : **Chayadevi M Bhamare**

Course Description

Introduction to embedded systems; embedded architectures; Architectures and programming of microcontrollers and DSPs; Embedded applications and technologies; power issues in system design; introduction to software and hardware co-design.

Scope and Objective of the course

The course covers the design issues involved in embedded systems and system-on-chip technologies. The course also deals with the applications and programming languages used for embedded systems.

Prescribed Text Books

- T1. Kamal, Raj, Embedded Systems: Architecture, Programming & Design, Tata McGraw Hill, 2nd Ed., 2008.
- T2. Valvano, Jonathan W, Embedded Microcomputer Systems, Real Time Interfacing, Cengage, 2nd Ed., 2007

Study Material

- SM 1. HC12 (CPU12) Reference Manual (**Access from the CD available with the book T2 in the directory \PDF\6812\cpu12rm.pdf**)
- SM 2. Motorola Semiconductor MC9S12C Family Data Sheet Rev. 1.15, July 2005 (**Access from the CD available with the book T2 in the directory \ PDF \ 6812 \ MC9S12C128_V1.pdf**)

Reference Books:

- R1. Jonathan W. Valvano, Introduction to Embedded Microcomputer Systems, Motorola 6811 and 6812 Simulation, (International Student Edition), Thomson Learning, 2003.
- R2. Wolf, Wayne, Computers as Components: Principles of Embedded Computing Systems Design, Elsevier, 2000.
- R3. Steven F. Barrett, Daniel J. Pack, Embedded Systems Design and Applications with the 68HC12 and HCS12, Pearson Education, 2005.
- R4. Sriram V Iyer, Pankaj Gupta, Embedded Realtime Systems Programming, TMH, 2004.

Plan of Self Study

Week No.	Topics	References to Text books	References to Study Materials for further reading / Additional Remarks
1.	INTRODUCTION Introduction to Embedded Systems. Hardware and Software Embedded Systems. Exemplary Embedded Systems – SOC.	T1-Chapter 1	Lecture Slides
2.	PROCESSOR AND MEMORY ORGANISATION Structural units in a processor and Processor Selection Memory Devices and Selection Direct Memory Access Interfacing Processor, Memories & I/O Devices	T1-Chapter 2	Lecture Slides
3.	DEVICES, DEVICE DRIVERS, BUSES I/O Devices, Timer and Counting Devices Device Drivers – Parallel and Serial Devices. Timing Devices Bus Architectures – I ² C, CAN, ISA, PC1, BDLC, Bluetooth	T1-Chapter 3	Lecture Slides
4.	INTERRUPTS Device Drivers and Interrupt Servicing Interrupt Servicing Mechanism, Context and Periods of Context Switching, Latency, Introduction to R705	T1-Chapter 4	Lecture Slides
5 & 6	Introduction to HC12 family, Processor Core Architecture, MC9S12C32 Features, Block Diagrams, Programming Models, Pinouts and Signals, System Clock.	T2-Chapter 1 (Sections 1.6, 1.8)	SM1- Section 1 & 2 SM2- Chapter 1 Sections 1.1.1 – 1.1.3, 1.3 (full), 1.4 (full).
	Register Blocks and Memory Mapping, Modes of Operation		SM2- Chapter 1 Sections 1.2 (full), 1.5 (full),
7 & 8	Addressing Modes and Assembly Language Programming	T2- Chapter 2 (Sections 2.1, 2.2, 2.3, 2.5, 2.10 & 2.11)	SM1- Section 3, 5 & 6
Syllabus for Mid-Semester Test (Closed Book): Topics covered in Week No. 1 to 8.			

Week No.	Topics	References to Text books	References to Study Materials for further reading / Additional Remarks
9	Resets and Interrupts, Watch Dog Timer, COP, Key-wakeup interrupts	T2- Chapter 4 (full) Chapter 3 (Section 3.2.3)	SM2- Chapter 1 Section 1.6(full), Chapters 5 & 9, Chapter 2 (sec 2.6)
10	Parallel I/O Ports, Internal and External Resource Mapping Control, (PIM + MMC + MEBI Modules)	T2- Chapter 1 (Section 1.9)	SM2- Chapters 2, 3 & 4
11 & 12	HC12 PERIPHERALS – I Parallel I/O Timer – Overflow, Output Compare, Input Capture, Pulse Accumulator PWM	T2- Chapter 2 (Sections 2.4.1, 2.4.3, 2.4.4, 2.4.5, 2.4.6) Chapter 6 (full) Chapter 8 (Sections 8.5 & 8.6)	SM2- Chapter 16 SM2- Chapter 13
13 & 14	HC12 PERIPHERALS – II Serial I/O SP1, SC1,	T2- Chapter 3 (Sections 3.6.1, 3.6.2, 3.6.4, 3.6.5) Chapter 7 (Sections 7.5, 7.6 & 7.7)	SM2- Chapters 14 & 15
	Analog to Digital Converters	T2- Chapter 11 (Sections 11.5-11.9, 11.10.2, 11.10.3)	SM2- Chapter 8
	CAN	T2- Chapter 14 (Sections 14.3 full)	SM2- Chapter 11
15 & 16	SYSTEM DESIGN Parallel Port and Memory Interfacing. Expanded Mode of Operation. System Design examples	T2- Chapter 8, 9 & 12 (Sections 8.1-8.3, 9.1-9.4, 9.5.1, 9.5.4, 9.6.2, 9.6.3, 12.5.full)	Involves all Chapters of SM1 & SM2 as listed in the plan of study.
Syllabus for Comprehensive Exam (Open Book): All topics given in the Plan of Self Study			
Note:			
<p>(1) (full) and x.x-x.x indicates all sections and subsections in that particular topic with respect to the MC9S12C32 microcontroller.</p> <p>(2) SM1 and SM2 should be used for reference purpose or when the relevant information is not available in the book T2.</p>			

Evaluation Scheme:

EC No.	Evaluation Component & Type of Examination	Duration	Weightage	Day, Date, Session, Time
EC-1	Assignment/Quiz	TBA	10%	TBA
EC-2	Mid-Semester Test (Closed Book)*	2 Hours	30%	Saturday, 03/09/2011 (FN)* 10 AM – 12 Noon
EC-3	Comprehensive Exam (Open Book)*	3 Hours	60%	Saturday, 29/10/2011 (FN)* 9 AM – 12 Noon

*** Legend:**

AN: AfterNoon Session; **FN:** ForeNoon Session; **TBA :** To be Announced

Closed Book Test: No reference material of any kind will be permitted inside the exam hall.

Open Book Exam: Use of any printed / written reference material (books and notebooks) will be permitted inside the exam hall. Loose sheets of paper will not be permitted. Computers of any kind will not be allowed inside the exam hall. Use of calculators will be allowed in all exams. No exchange of any material will be allowed.

Note:

It shall be the responsibility of the individual student to be regular in maintaining the self study schedule as given in the course handout, attend the online/on demand lectures as per details that would be put up in the BITS WILP website www.bits-pilani.ac.in/dlp-home and take all the prescribed components of the evaluation such as Mid Semester Test and Comprehensive Examination according to the Evaluation Scheme given in the respective Course Handout. If the student is unable to appear for the Regular Test/Examination due to genuine exigencies, the student must refer to the procedure for applying for Make-up Test/Examination, which will be available through the **Important Information** link on the BITS WILP website on the date of the Regular Test/Examination. The Make-up Tests/Exams will be conducted only at selected exam centres on the dates to be announced later.

Instructor-in-Charges