27th International Symposium on VLSI Design and Test (VDAT-2023)
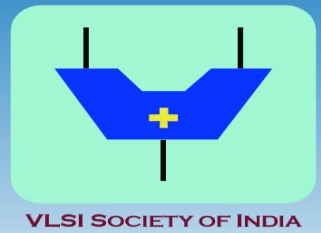
Sept. 29 - Oct. 01, 2023
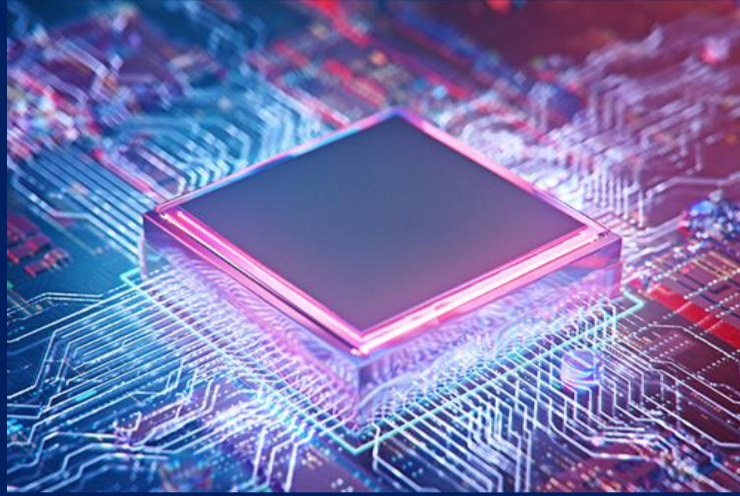
BITS Pilani — Pilani Campus

CSIR-CEERI Pilani

G20 भारत 2023 INDIA

VLSI SOCIETY OF INDIA

SYMPOSIUM VENUE → BITS Pilani - Pilani Campus (Rajasthan) 333 031, INDIA

CALL FOR PAPERS

VLSI Design & Test Symposium (VDAT) promotes research and development in various fields of VLSI Design. VDAT began as a small workshop in the year 1998, and in 2005 it acquired the status of an international symposium. The 27th International Symposium on VLSI Design and Test (VDAT-2023) will be jointly hosted by Birla Institute of Technology & Science (BITS), Pilani, and CSIR - Central Electronics Engineering Research Institute (CSIR-CEERI), Pilani. This symposium aims to bring Industries, Academics, Researchers, Startups, MSMEs, and related practitioners together to exchange their ideas for leveraging in their respective fields. The VLSI Society of India, leading institutes and industries actively support the symposium.

Emerging Chip Architectures for Future: Beyond Moore's Law

Low-Power Integrated Circuits and Devices
- Low-Power Analog/Digital/Mixed Signal Circuits
- Low-Voltage Low-Power Sensors Interface
- Circuit design for Reliability
- Device Modelling and Simulation
- MEMS/NEMS/MOEMS Devices, Organic Devices

FPGA-based Design and Embedded Systems
- Adaptive Computing using Reconfigurable Fabrics
- Large-Scale Systems and Power Networks
- Hardware-Software Co-design
- Reconfigurable and FPGA-based Design
- Multi-FPGA Systems

Memory, Computing & Processor Design
- Memory Design
- STT-RAM, PC-RAM, R-RAM, and Memristors
- Emerging Memory Technologies
- Neuromorphic Computing
- Quantum Computing

System-Level Design
- Systems-on-Chip (SoC), Lab-on-Chip
- Mixed-Mode System-on-Chip
- High-Speed Interconnects, Network-on-Chip
- Wireless Transceivers, Multimedia Processors
- Heterogeneous and Homogeneous MPSoCs

VLSI Architectures and System Integration
- VLSI Processors & Signal Processing Architectures
- RF Integrated Circuits & Systems
- Machine Learning Architectures
- Low-Power IoT Architectures and Systems
- Compressive Sensing, Wireless Systems

Emerging Integrated Circuits and Systems
- Artificial Intelligence Accelerators
- Cognitive Computing Systems
- Printed & Flexible Electronics
- Low Power Edge Computing System
- Analog/Digital/Mixed Signal Circuits

VLSI Testing and Security
- Hardware Security and VLSI Design Optimization
- Hardware Attacks, Detection, Threat Modelling
- Fault Diagnosis and Fault Models
- DFT and BIST for Digital Designs

CAD for VLSI
- Design Automation and CAD Tools
- Design Flows for MPSoCs
- ML/AI based Design-Flows and EDA
- Design Automation for DFX

Student Fellowship
VDAT-2023 will provide a limited number of fellowships to Undergraduate and Masters students for attending the symposium. Details may be checked out from the website.

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Dates & Deadlines (Extended)

Regular Papers
Full Paper Submission: ~~June 15, 2023~~ June 25, 2023
Notification of Acceptance: ~~July 22, 2023~~ July 31, 2023
Camera Ready Paper: ~~August 07, 2023~~ August 10, 2023

Tutorials
Tutorial Proposal Submission: ~~June 15, 2023~~ June 30, 2023
Tutorial Announcement: ~~August 15, 2023~~ August 15, 2023

Poster Papers
Paper Submission: ~~June 15, 2023~~ June 25, 2023
Notification of Acceptance: ~~July 22, 2023~~ July 31, 2023
Camera Ready Paper: ~~August 07, 2023~~ August 10, 2023

Design Contest
Submission of Design: ~~June 15, 2023~~ July 31, 2023
Notification of Acceptance: ~~July 22, 2023~~ August 31, 2023

A Push for Aatma Nirbhar Bharat

Submission Guidelines
Authors are invited to submit original, unpublished research manuscripts on the above topics. Submissions must be done through easy-chair portal. All papers will be reviewed by at least three members of the program committee, with a double-blind review process. Soft copies of papers should be submitted in PDF format, manuscripts should not exceed six A4 size pages and should be uploaded online. All accepted papers must be presented by one of the authors in order to be included in the **SCOPUS** indexed **Springer CCIS** conference proceedings.

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