Day 1: Sept 29, 2023 (Friday)

07:45-09:00	**Registration** Lecture Theater Complex (LTC)									
09:00-11:00	**Tutorial-1 (LTC-5102)** ASIC Design Flow Mr. Sunil Nanda, Ex-Nvidia									
11:00-11:30	**Tea Break**									
11:30-13:30	**Tutorial-2 (LTC-5102)** VLSI Architecture Design: Concepts & Choices Architectural Exploration and High-Level Synthesis in Automotive VLSI Systems Prof. Chandra Shekhar and Dr. Prateek Sikka									
13:30-14:30	**Lunch Break**									
14:30-16:00	**Tutorial -3 (LTC-5102)** Basics of Design for Test and Diagnosis, Cadence									
16:00-16:30	**Tea Break**									
16:30-18:00	**Tutorial-4 (LTC-5102)** Pushing the Limits of Semiconductor Scaling Cadence						**Tutorial-5 (LTC-5105)** MBIST Implementation of Shared Bus Interface Integrated Memories eInfochips			
18:00-18:30	**COFFEE with MICRON: A Student Interaction**									
20:00-21:00	**Dinner**									

Day 2: Sept 30, 2023 (Saturday)

07:30-09:15	**Registration (Lecture Theater Complex (LTC))**									
09:15-09:45	Inauguration Function VDAT-2023 (Venue: LTC-5105) Address by Prof. V Ramgopal Rao, Vice-Chancellor, BITS, Pilani Address by Prof. Sudhirkumar Barai, Director, BITS, Pilani Address by Dr. P. C. Panchariya, Director, CSIR-CEERI, Pilani Address by Prof. Chandra Shekhar, General Chair, VDAT-2023 Address by Prof. M Balakrishnan, General Chair, VDAT-2023 Address by Dr. Satya Gupta, President, VSI									
09:50-10:30	**Keynote – I (LTC-5105)** **Memories at the Heart of Intelligent Systems** Anand Ramamoorthy, Micron Technology									
10:40-11:10	**Tea Break**									
11:10-12:00	**Keynote – II (LTC-5105)** **Verification Challenges for Next Generation Automotive and AI Designs** Apoorwa Kapse, Marvell Technology									
12:00-13:30	**Paper Presentation: Session 1 (LTC-5104)** **Analog**			**Paper Presentation: Session 2 (LTC-5105)** **Digital**			**Paper Presentation: Session 3 (LTC-5102)** **Devices**			
	1.1	170	Analysis of SQNR Degradation in Noise-Shaped SAR Analog-to-Digital Converters at High Input Signal Amplitudes	2.1	84	A Hybrid Approximate Adder for Energy-efficient Computing	3.1	185	Analysis and Modeling of Self Heating and Substrate Induced Transitions in 5 nm Stacked Nanosheet FET	
	1.2	38	An improved clock booster circuit suitable for boost converters in energy harvesting environments	2.2	142	Energy Harvester Powered Fully Digital ECG Front End Acquisition with Integrated TDC	3.2	73	Optimization of sol-gel TiO2 thin films for photovoltaic organic photodetector	
	1.3	30	A 0.1-4.71GHz Integer-N CP-PLL Based Low Power Frequency Synthesizer for High Speed Applications	2.3	181	An Energy Efficient Mixed Logic 2-to-4 Decoder for Embedded Memory Applications	3.3	133	Role of solvents on the performance of bulk heterojunction (BHJ) organic solar cells	
	1.4	154	A Comprehensive Design and Analysis of a Dual-output Filter and A Novel Triple-output Current-mode Filter for RF Applications	2.4	76	Electrically-Tunable Fractional-Order Universal Filter	3.4	136	Chemisorption Analysis of NOx Sensor Using NF/Pr-AGNR: A DFT Investigation	
	1.5	49	A Current-Mode-Logic Based PFD-Charge Pump Circuit for Low Reference Spur PLLs	2.5	129	Power Efficient Approximate Multiplier for Neural Network Applications	3.5	46	Design and Analysis of Differential Configuration based Active Inductor for 5G Sub-6GHz Applications	
13:30-14:30	Lunch Break									
14:30-15:10	**Invited Talks – I (LTC-5105)** **Generative AI for IoT Systems** Prof. Santanu Chaudhury, Director IIT Jodhpur									
15:10-15:50	**Invited Talks – II (LTC-5105)** **ASIC/SOC design methodologies and AI assisted design** Subhash Chintamaneni, Micron Technology									
15:50-16:20	**Tea Break**									
16:20-17:50	**Paper Presentation: Session 4 (LTC-5104)** **Analog**			**Paper Presentation: Session 5 (LTC-5105)** **Digital**			**Paper Presentation: Session 6 (LTC-5102)** **Devices**			
	4.1	176	Parallel Feedback Controlled Low-Power and Reliable Schmitt Trigger Circuit	5.1	167	Robust and High Performance Digital In-Memory Computing in 5T Gain Cell Embedded DRAM	6.1	67	Demonstration of Doped-HfO2 Ferroelectric based Double Layer Stacked NC FinFET	
	4.2	63	A Low Jitter and High Speed Flash TDC with PVT Calibration and its Testing Methodology	5.2	110	Enhancing the Accuracy and Resource Utilization of Field Programmable CRC circuit architecture	6.2	69	Indexed Fin Grids based Methodology to Address Process Variation Challenges of Self-Aligned Quadruple Patterning	
	4.3	74	A Dual-Mode High-Frequency Grounded Memristor Emulator Circuit	5.3	145	AFX-PE: Adaptive Fixed-Point Processing Engine for Neural Network Accelerators	6.3	200	High Precision Programmable Thermistor Linearization ASIC for Electro-Optical Payload Applications	
	4.4	39	Analysis and Reduction of GOTFET Capacitances Using Physics-Based Compact Modeling	5.4	152	Optimized Composite Field Based Hardware Architectures for AES S-box using Logic Decomposition Techniques	6.4	107	Microwave Assisted ultrafast Synthesis of Fe3O4 Based Memristor for Neuromorphic System	
	4.5	148	A Fast Transient Low Iq Capless LDO with Protection Circuits	5.5	31	SPEEDY : SystemC Based Design Space Exploration Framework for Embedded Systems	6.5	92	Current-Sensing ADC with power consumption of 57nW and FoM of 336 fJ/conversion at 28nm CMOS technology	
18:30-19:15	**Brain Storming Panel-I: Semiconductor Ecosystem for a Push Towards Aatma Nirbhar Bharat**									
	Prof. V Ramgopal Rao, Prof. Chandra Shekhar, Prof. M. Balakrishnan, Prof. G S Visweswaran, Prof. Dinesh Sharma, Dr. Satya Gupta, Ms. Chitra Hariharan									
19:30-22:00	**Banquet Talk & Dinner**									

Day 3 Oct. 01, 2023 (Sunday)

07:30-09:15	**Registration (Lecture Theater Complex (LTC))**									
09:15-09:55	**Invited Talk – III (LTC-5105)** **Role of Advanced Memory Technology in Emerging Technologies** Partha Parthasarathy, Micron Technology									
10:00-10:40	**Invited Talk – IV (LTC-5105)** **RF IV Characterization** Mr Vishal Gupta, Keysight Technologies									
10:40-11:10	**Tea Break**									

11:15-13:00	**Paper Presentation: Session 7 (LTC-5104)**			**Paper Presentation: Session 8 (LTC-5105)**			**Paper Presentation: Session 9 (LTC-5102)**		
	Analog			**Architectures**			**Security_Emerging**		
	7.1	127	Design and Analysis of Low-Power Protection Circuits for LDO Regulators	8.1	58	B-box: An Efficient and Configurable RISC-V Bit Manipulation IP Generator	9.1	54	A 2D transformation technique for Nearest Neighbor Realization of Quantum Circuits
	7.2	172	Comparative study of FET based biosensors with metal oxide stacked sensing membrane	8.2	90	CoDriVer: A Tool for Coverage-driven Functional Verification of RISC-V Processors	9.2	166	LightLock: Ensuring Hardware IP Security in IoT Environment with Lightweight Logic Locking
	7.3	81	Preventing Costly Iterations by Delivering SoC Congestion Aware Standard Cell Lib using Pin Accessibility Checker	8.3	195	FPGA Implementation of Resource-Efficient Cube Calculation Architecture using Yavadunam Sutra	9.3	79	Indigenous Development of SPARC Processor based Radar Controller (SPRC) ASIC
	7.4	150	A 0.076-mW 9.8-ENOB 1-MS/s SAR ADC using novel R-C hybrid DAC	8.4	37	High Throughput Multiple Device Diagnosis System for Hierarchical Test Designs	9.4	171	A Walkthrough of Reconfigurable SV-UVM based MIPI Standard UniPro2.0 IP DV Test bench: Challenges and Approaches
	7.5	48	Efficient 1-bit Hybrid Full Adder Design with Low Power Delay Product using FinFET-TGDI Technology: Simulation and Comparative Study	8.5	196	A Hybrid BAT Algorithm for Scheduling Droplet Mixing Operations in Digital Microfluidic Biochips	9.5	72	Reducing layout design cycle iterations by resizing and spitting electrically violated pins by push button
13:30-14:30	**Lunch Break**								
14:30-15:20	**Invited Talk V (LTC-5105)**								
	Low Power Test Sequence Generation for Robust Testable PDF								
	Prof. Anzhela Matrosova								
15:30-16:45	**Paper Presentation: Session 10**			**Paper Presentation: Session 11**			**Paper Presentation: Session 12**		
	Analog (LTC-5104)			**Security (LTC-5105)**			**Emerging Fields (LTC-5102)**		
	10.1	182	Characterization of Multi-Vt Transistors for Analog IC Design in Sub-nanometer Technologies	11.1	123	An Efficient Hardware Implementation of Elliptic Curve Point Multiplication over GF(2^m) on FPGA	12.1	86	Accuracy Reconfigurable Carry Bypass Approximate Adder as Co-processor to RISC V
	10.2	141	AlN/β-Ga2O3 HEMT For Low Noise Amplifier	11.2	190	Test Vector Generation for Detecting Hardware Trojan using Machine Learning Approaches	12.2	183	A NAND Flash Memory Controller for Energy-Constrained Edge Computing Applications
	10.3	85	Design and Analysis of Modified Strong Arm Latch Comparator with Reduced Kickback Noise	11.3	75	An Optimized Hardware Implementation of ASCON Cipher for IoT Applications	12.3	177	A Test Generation Approach for Spiking Neural Network Simplification
	10.4	61	Construction of non-rectangular floor plans for properly triangulated planar graphs	11.4	119	A High-Speed Bitwise Computation in SRAM using Assisted Bitline Charging/Discharging	12.4	197	Approach Towards In-Memory Computing Based Hamming Code Implementation for Error Correction and Detection
16:45-17:00	**Tea Break**								
17:00-17:30	Travel to CEERI								
17:30-18:30	**Brain Storming Panel-II: Semiconductor Ecosystem for a Push Towards Aatma Nirbhar Bharat, CSIR-CEERI**								
	Dr. V Ramgopal Rao, Dr. P. C. Panchariya, Dr. Chandra Shekhar, Dr. M. Balakrishnan, Prof. G S Visweswaran, Prof. Dinesh Sharma & Others								
18:30-19:00	**Valedictory Function: Award and Certificate Ceremony**								
19:15-20:00	**Technology Display from CEERI**								
20:00-22:00	**Dinner**								